



2183
[Signature]

Docket No. 114596-28-0053BS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): John S. Yates Jr., et al.

Serial No.: 09/626,325

Art Unit: 2183

Filed: July 26, 2000

Examiner: R. Ellis

Title: OPERATING SYSTEM FOR COMPUTER WITH TWO ARCHITECTURES

CERTIFICATE OF MAILING (37 C.F.R. § 1.8a)

Mailstop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I hereby certify that the attached

- Return postcard
- This Certificate of Mailing
- Information Disclosure Statement
- Form PTO -1449
- 10 References

along with any paper(s) referred to as being attached or enclosed) and this Certificate of Mailing are being deposited with the United States Postal Service on date shown below with sufficient postage as first-class mail in an envelope addressed to the: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Respectfully submitted,

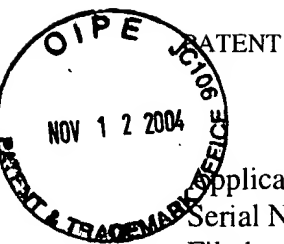
WILLKIE FARR & GALLAGHER, LLP

Dated: November 9, 2004

By: *[Signature]*

David E. Boundy
Registration No. 36,461

Mailing Address:
WILLKIE FARR & GALLAGHER, LLP
787 Seventh Ave.
New York, New York 10019
(212) 728-8000
(212) 728-8111 Fax



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): John S. Yates Jr., et al.

Serial No.: 09/626,325

Art Unit: 2183

Filed: July 26, 2000

Examiner: R. Ellis

Title: OPERATING SYSTEM FOR COMPUTER WITH TWO ARCHITECTURES

INFORMATION DISCLOSURE STATEMENT

Mailstop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In accordance with 37 C.F.R. §§1.56, 1.97 and 1.98, Applicant wishes to make of record the items listed on the accompanying Form PTO-1449. Applicant respectfully requests the Examiner to fully consider the items and independently ascertain their teaching before issuance of the next action, and to make them of record in the file. The Examiner is also requested to initial and return a copy of the enclosed Form PTO-1449 to evidence such consideration.

The references listed on the enclosed Form 1449 have come to light in applications listed in the Information Disclosure Statement of November 2000. Applicant has not reviewed all of them in detail. Of those that have been reviewed, none of the references are believed to be any more pertinent than the references provided in earlier IDS' and Forms 1449. However, in an abundance of caution, Applicant requests that they be considered.

Several of these references have already been considered. They are presented again here for one or more of the following reasons: (a) to place them in this file to improve convenience of examination of applications that claim priority from this application, or (b) to supplement the bibliographic information previously provided.

For non-patent items listed on the enclosed Form PTO-1449 for which a copy is not already made of record in this application, a copy was previously cited by or submitted to the Patent and Trademark Office in application Serial No. 09/239,194, filed January 28, 1999, Yates et al., Executing Programs for a First Computer Architecture on a Computer of a Second

I certify that this correspondence, along with any documents referred to therein, is being deposited with the United States Postal Service on November 9, 2004 as First Class Mail in an envelope with sufficient postage addressed to The Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450..

Architecture, in application Serial No. 09/322,443, filed May 28, 1999, Reese et al., Profiling of Computer Programs Executing in Virtual Memory Systems, or in application Serial No. 09/385,394, filed August 30, 1999, Yates et al., Computer for Executing Two Different Instruction Sets.

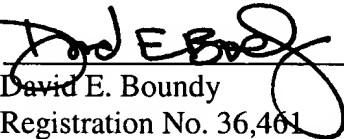
This Information Disclosure Statement it is being filed at a time when prosecution is closed but may be reopened. In the event of reopening, entry of this IDS is proper. In that event, a fee will be due pursuant to 37 C.F.R. §1.97(c)(2), to be charged to Deposit Account 23-2405, Order No. 114596-28-0053BS.

The Commissioner is hereby authorized to charge any additional fees that may be required for this Information Disclosure Statement, or credit any overpayment, to Deposit Account 23-2405, Order No. 114596-28-0053BS.

Respectfully submitted,

WILLKIE FARR & GALLAGHER, LLP

Dated: November 9, 2004

By: 
David E. Boundy
Registration No. 36,461

Mailing Address:
WILLKIE FARR & GALLAGHER, LLP
787 Seventh Ave.
New York, New York 10019
(212) 728-8000
(212) 728-8111 Fax

09/626,325

John S. Yates Jr., et al.

July 26, 2000

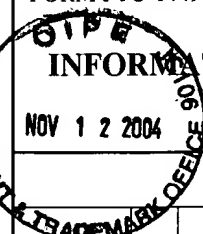
2183

(Use several sheets if necessary)

NOV 12 2004

U.S. PATENT DOCUMENTS

[illegible]**DATE CONSIDERED**

FORM PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. 114596-28-0053BS	SERIAL NO. 09/626,325
 INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)				APPLICANT John S. Yates Jr., et al.	
				FILING DATE July 26, 2000	GROUP ART UNIT 2183
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Papers, Etc.)					
			Brad Calder, Peter Feller, Alan Eustace, Value Profiling, Proceedings of 30th International Symposium on Microarchitecture (Micro-30), IEEE, pages 259-269 (December 1-3, 1997)		
			Compaq Computer Corp., Compiler Writer's Guide for the Alpha 21264 (1999) www.alphalinux.org/archives/axp-list/June1999/0475.html		
			Dean, ProfileMe: Hardware Support for Instruction-Level Profiling on Out-of-Order Processors," Proceedings of 30th Annual Intl. IEEE/ACM Symp. on Microarchitecture, pp. 292-302 (Dec. 1997)		
			Digital Equipment Corp., White Paper: How DIGITAL FX!32 Works (September 1997) http://www.digital.com/semiconductor/amt/fx32/fx-white.htm		
			Linda Geppert et al., Transmeta's Magic Show, IEEE Spectrum, vol. 37 no. 5, pp. 26-33 (May 2000)		
			Kavi et al., A Performability Model for Soft Real-Time Systems, IEEE Proceedings of the 27th Annual Hawaii International Conference on System Sciences, pp. 571-579 (1994)		
			Kim and Tyson: Analyzing the Working Set Characteristics of Branch Execution, Proceedings of the 31st Annual ACM/IEEE International Symposium on Microarchitecture, pp. 49-58 (Dec. 1998)		
			Monica S. Lam, Robert P. Wilson, Limits of Control Flow on Parallelism, Proceedings of the 19th Annual International Symposium on Computer Architecture, p.46-57 (May 1992)		
			Larus and Schnarr: EEL: Machine-Independent Executable Editing, EEL: Machine-independent executable editing. In Proceedings of the ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI), 1995		
			M. Lipasti and J. Shen. Exceeding the Data-Flow Limit Via Value Prediction, 29th International Symposium on Microarchitecture, pages 226-237, IEEE (Dec. 1996)		
			Veen: Dataflow Machine Architecture, ACM Computing Surveys vol. 18 no. 4 pp. 365-96 (December 1986)		
EXAMINER			DATE CONSIDERED		